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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re application of: Subir Ghosh

and Hsu-Tien Tung

Application No.: 10/619,798

Filed: July 15, 2003

Title: PREDICTIVE SNOOPING OF CACHE

MEMORY FOR MASTER-INITIATED

ACCESSES

Attorney Docket No.: **OPTI 3140-6**

Examiner: ELLIS, Kevin L.

Group: 2188

Confirmation No.: Not Known

Customer No. 22470

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

United States Patent and Trademark Office Customer Service Window Randolph Building 401 Dulany Street Alexandria, VA 22314

Sir:

It is requested that the information identified in this statement be considered by the Examiner and made of record in the above-identified application. This statement is not intended to represent that a search has been made or that the information cited in the statement is, or is considered to be, material to patentability as defined in 37 C.F.R. 1.56.

Since this is a continuation, divisional or continuation-in-part application, it is understood that the Examiner will consider all information which was considered by the Office in a parent application. MPEP 609.

Application No.: 10/619,798

Attorney Docket No. OPTI 3140-6

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Enclosed with this statement is a Form PTO/SB/08A. The Examiner is requested to initial the form and return it to the undersigned in accordance with M.P.E.P. 609.

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This statement should be considered under 37 C.F.R. 1.97(b) because it is being filed before the mailing date of the first Office Action after the filing of a Request for Continued Examination under 37 C.F.R. 1.114.

Fee Authorization. The Commissioner is hereby authorized to charge underpayment of any additional fees or credit any overpayment associated with this communication to Deposit Account No. 50-0869 (OPTI 3140-6). A duplicate copy of this authorization is enclosed.

Respectfully submitted,

Haynes Beffel & Wolfeld LLP

Date: November 23, 2005

Warren S. Wolfeld, Reg. No. 31,454

Haynes Beffel & Wolfeld LLP P.O. Box 366; 751 Kelly Street Half Moon Bay, CA 94019 Ph. (650) 712-0340 Fax (650) 712-0263

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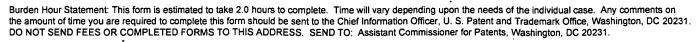
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				Application Number	10/619,798			
NFC	DRMATI	ON DISC	CLOSURE	Filing Date	15 July 2003			
STATEMENT BY APPLICANT			PLICANT	First Named Inventor	Subir Ghosh			
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	(use as ma	any sheets as n	necessary)	Examiner Name	ELLIS, Kevin L.			
eet	-1	of	3	Attorney Docket Number	OPTI 3140-6			

	, .	OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS	_
examiner nitials	Cite No. ¹	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T
	C1	MOTOROLA INC., "PowerPC 601 RISC Microprocessor Technical Summary", Freescale Semiconductor, Inc., 1993	
	C2	NORMAN P. JOUPPI, "Improving Direct-Mapped Cache Performance by the Addition of a Small Fully-Associative Cache and Prefetch Buffers, 18 Computer Architecture News 364-373, 1990	
•	C3	NORMAL P. JOUPPI, "Reducing Compulsory and Capacity Misses", WRL Technical Note TN-53, August 1990	
	C4	FREDRIK DAHLGREN ET AL., "Sequential Hardware Prefetching in Shared-Memory Multiprocessors", 6 IEEE Transactions on Parallel and Distributed Systems 733-746, 1995	
·	C5	DEAN M. TULLSEN, SUSAN J. EGGERS, "Limitation of Cache Prefetching on a Bus-Based Multiprocessor", Proceedings of the 20th Annual International Symposium on Computer Architecture at 278-88, 1993	
	C6	WILLIAM Y. CHEN ET AL., "Data Access Microarchitectures for Superscalar Processors with Compiler-Assisted Data Prefetching", Proceedings of the 24th Annual International Symposium on Microarchitecture at 69-73, 1991	
	C7	ALAN JAY SMITH, "Cache Memories", 14 ACM Computing Surveys 473-530, 1982	
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	C9	TIEN-FU CHEN & JEAN-LOUP BAER, "Effective Hardware-Based Data Prefetching for High Performance Processors, 44 IEEE Transactions on Computer 609-623, May 1995	
	C10	TIEN-FU CHEN & JEAN-LOUP BAER, "A Performance Study of Software and Hardware Prefetching", 22 Computer Architecture News 223-232, 1994	
	C11	TIEN-FU CHEN & JEAN-LOUP BAER, "Reducing Memory Latency via Non-blocking and Prefetching Caches", Fifth International Conference on Architectural Support for Programming Languages and Operating Systems at 51-61, 1992	

Examiner	Date	
Signature	Considered	

¹ Unique citation designation number. ² Applicant is to place a check mark here if English language Translation is attached.



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Substitu	Substitute for form 1449B/PTO			Complete if Known				
				Application Number	10/619,798			
INFO	ORMATION	4 D	ISCLOSURE	Filing Date	15 July 2003			
STATEMENT BY APPLICANT				First Named Inventor	Subir Ghosh			
0.,			/	Group Art Unit	2188			
	(use as many s	sheets	s as necessary)	Examiner Name	ELLIS, Kevin L.			
Sheet	2	of	3	Attorney Docket Number	OPTI 3140-6			

		OTHER PRIOR ART – NON PATENT LITERATURE DOCUMENTS	
Examiner Initials*	Cite No.1	Include name of the author (in CAPITAL LETTERS), title of the article (when appropriate), title of the item (book, magazine, journal, serial, symposium, catalog, etc.), date, page(s), volume-issue number(s), publisher, city and/or country where published.	T²
	C12	LUCIEN CENSIER & PAUL FEAUTRIER, "A New Solution to Coherence Problems in Multicache Systems", 27 IEEE Transactions on Computers 1112-1118, 1978	
	C13	MICHEL DUBOIS ET AL., "Memory Access Buffering in Multiprocessors", 14 Computer Architecture News 434-442, 1986	
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		ISCLOSURE	Filing Date	15 July 2003				
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(use as many sheets as necessary)				Examiner Name	ELLIS, Kevin L.			
Sheet	3	of	3	Attorney Docket Number	OPTI 3140-6			

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	C23	TIEN-FU CHEN, "Data Prefetching for High-Performance Processors (July 1993) (Ph.D. Thesis, University of Washington)							
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